

| | | | | | | | |
|--|---|---|----------------------|-------------------------|---------------------------|----------------------------|-------------|
| FORM PTO-892 | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | SERIAL NO. 09/159748 | GROUP ART UNIT 2123 | ATTACHMENT TO PAPER NO. | 4 |
| NOTICE OF REFERENCES CITED | | | | APPLICANT(S) Barrett | | | |
| U.S. PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | NAME | CLASS | SUB-CLASS | FILING DATE |
| | A | 5,937,183 | 8/1999 | Ashar et al | 703 | 15 | |
| | B | 5,748,486 | 5/1998 | Ashar et al | 716 | 18 | |
| | C | 5,522,063 | 5/1996 | Ashar et al. | 716 | 4 | |
| | D | 5,477,474 | 12/1995 | Southgate et al. | 703 | 15 | |
| | E | 5,469,367 | 11/1995 | Puri et al. | 716 | 18 | |
| | F | 5,640,328 | 6/1997 | Lam | 716 | 8 | |
| | G | 6,086,626 | 7/2000 | Jain et al. | 716 | 5 | |
| | H | 5,649,165 | 7/1997 | Jain et al. | 716 | 5 | |
| | I | 5,668,732 | 9/1997 | Khouja et al. | 702 | 60 | |
| | J | 6,035,107 | 3/2000 | Kuehlmann et al. | 716 | 18 | |
| | K | | | | | | |
| FOREIGN PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | COUNTRY | NAME | CLASS | SUB-CLASS |
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |
| | O | | | | | | |
| | P | | | | | | |
| | Q | | | | | | |
| OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | |
| | R | "Dynamic Minimization of OKFDDs", Drechsler et al., IEEE 1995. | | | | | |
| | S | "Representation of Switching Circuits by Binay-Decision Programs", Lee, The Bell System Technical Journal, July 1959. | | | | | |
| | T | "Binary Decision Digrams", IEEE 1978. | | | | | |
| | U | "Graph-Based Algorithms for Boolean Function Manipulation", Bryant, IEEE 1986. | | | | | |
| EXAMINER W Thomson | | | DATE May 30, 2002 | | Form892ccs2106b | | |
| * A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).) | | | | | | | |

| | | | | | | | |
|--|---|---|-----------------------------|------------------------------------|----------------------------------|----------------------------|----------------|
| FORM PTO-892 | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | SERIAL NO. 09/159748 | GROUP ART UNIT 2123 | ATTACHMENT TO PAPER NO. | 4 |
| NOTICE OF REFERENCES CITED | | | | APPLICANT(S) Barrett | | | |
| U.S. PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | NAME | CLASS | SUB- CLASS | FILING DATE |
| | A | | | | | | |
| | B | | | | | | |
| | C | | | | | | |
| | D | | | | | | |
| | E | | | | | | |
| | F | | | | | | |
| | G | | | | | | |
| | H | | | | | | |
| | I | | | | | | |
| | J | | | | | | |
| | K | | | | | | |
| FOREIGN PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | COUNTRY | NAME | CLASS | SUB- CLASS |
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |
| | O | | | | | | |
| | P | | | | | | |
| | Q | | | | | | |
| OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | |
| | R | "The Size of Reduced OBDD's and Optimal REad-One Branching Programs for Almost All Boolean Functions", Wegener, IEEE 1994. | | | | | |
| | S | "Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams", Bryant, ACM 1992. | | | | | |
| | T | "Efficient Implementation of a BDD Package", Brace et al., IEEE 1990. | | | | | |
| | U | "On the Complexity of VLSI Implementations and Graph Representations of Boolean Functions with Application to Integer Multiplication", Bryant, IEEE 1991. | | | | | |
| EXAMINER W Thomson | | | DATE May 30, 2002 | | Form892ccs2106b | | |
| * A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).) | | | | | | | |

| | | | | | | | |
|--|---|--|-----------------------------|------------------------------------|----------------------------------|--|-------------|
| FORM PTO-892 | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | SERIAL NO. 09/159748 | GROUP ART UNIT 2123 | ATTACHMENT TO PAPER NO. 4 | |
| NOTICE OF REFERENCES CITED | | | | APPLICANT(S) Barrett | | | |
| U.S. PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | NAME | CLASS | SUB-CLASS | FILING DATE |
| | A | | | | | | |
| | B | | | | | | |
| | C | | | | | | |
| | D | | | | | | |
| | E | | | | | | |
| | F | | | | | | |
| | G | | | | | | |
| | H | | | | | | |
| | I | | | | | | |
| | J | | | | | | |
| | K | | | | | | |
| FOREIGN PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | COUNTRY | NAME | CLASS | SUB-CLASS |
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |
| | O | | | | | | |
| | P | | | | | | |
| | Q | | | | | | |
| OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | |
| | R | "Logic Verification using Binary Decision Diagrams in a Logic Synthesis Environment", Malik et al., IEEE 1988. | | | | | |
| | S | "Evaluation and improvement of Boolean comparison method based on binary decision diagrams", Fujita et al., IEEE 1988. | | | | | |
| | T | "On Variable Ordering of Binary Decision Diagrams for the Application of Multi-level Logic Synthesis", Fujita et al., IEEE 1991. | | | | | |
| | U | "Interleaving Based Variable Ordering Methods for Ordered Binary Decision Diagrams", Fujii et al., IEEE 1993. | | | | | |
| EXAMINER W Thomson | | | DATE May 30, 2002 | | Form892ccs2106b | | |
| * A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).) | | | | | | | |

| | | | | | | | |
|--|---|---|-----------------------------|------------------------------------|----------------------------------|----------------------------|----------------|
| FORM PTO-892 | | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | SERIAL NO. 09/159748 | GROUP ART UNIT 2123 | ATTACHMENT TO PAPER NO. | 4 |
| NOTICE OF REFERENCES CITED | | | | APPLICANT(S) Barrett | | | |
| U.S. PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | NAME | CLASS | SUB- CLASS | FILING DATE |
| | A | | | | | | |
| | B | | | | | | |
| | C | | | | | | |
| | D | | | | | | |
| | E | | | | | | |
| | F | | | | | | |
| | G | | | | | | |
| | H | | | | | | |
| | I | | | | | | |
| | J | | | | | | |
| | K | | | | | | |
| FOREIGN PATENT DOCUMENTS | | | | | | | |
| * | | DOCUMENT NO. | DATE | COUNTRY | NAME | CLASS | SUB- CLASS |
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |
| | O | | | | | | |
| | P | | | | | | |
| | Q | | | | | | |
| OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | |
| | R | "Breadth-First Manipulation of Very Large Binary-Decision Diagrams", OCHI et al., IEEE 1993. | | | | | |
| | S | "Novel Verification Framework Combining Structural and OBDD Methods in a Synthesis Environment", Reddy et al., ACM/IEEE 1995. | | | | | |
| | T | "Minimizing ROBDD sizes of incompletely specified Boolean functions by exploiting strong symmetries", Scholl et al., IEEE March 1997. | | | | | |
| | U | "Linear Sifting of Decision Diagrams", Meinel et al., IEEE June, 1997. | | | | | |
| EXAMINER W Thomson | | | DATE May 30, 2002 | | | | |
| Form892ccs2106b | | | | | | | |
| * A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).) | | | | | | | |